

CLAIMS

What is claimed is:

1           1.    A method of constructing an accumulator,  
2 comprising:  
3           simulating a layered tree structure, said structure  
4 configured to contain intermediate result data during  
5 accumulation; and  
6           programming said structure to direct said result data  
7 and to direct initial inputs from an arbitrary length  
8 string such that said accumulator maintains the order of  
9 operations within each simulated layer.

1           2.    A method according to claim 1 wherein simulating  
2 includes:  
3           implementing said layered tree structure by including  
4 a left memory bank and a right memory bank for every  
5 operational layer of said layered tree structure.

1           3.    A method according to claim 2 wherein said  
2 implementing further includes:  
3           segregating said left memory bank into FIFOs, the  
4 FIFOs one more than the number of operational layers  
5 desired in said layered tree being simulated.

1           4.    A method according to claim 2 wherein said  
2   implementing further includes:  
3           segregating said right memory bank into FIFOs, the  
4   FIFOs equal to the number of operational layers desired in  
5   said layered tree being simulated.

1           5.    A method according to claim 1 further comprising:  
2           utilizing a single adder and control device to perform  
3   adds of all layers of said layered tree structure.

1           6.    A method according to claim 5 further comprising:  
2           providing a left source to said adder and control  
3   device; and  
4           providing a right source to said adder and control  
5   device.

1           7.    A method according to claim 6 wherein said left  
2   source and said right source are summed by said adder and  
3   control device, the result thereof directed to one of said  
4   left memory bank, said right memory bank and a result  
5   queue.

1           8.    A method according to claim 6 wherein said left  
2 source is selected from among data of said left memory bank  
3 and one said initial input.

1           9.    A method according to claim 8 wherein said right  
2 source is selected from among data of said right memory  
3 bank and one said zero value.

1           10.   A method according to claim 9 wherein said left  
2 and right sources are accompanied by control fields which  
3 control the flow of data, said control fields including, a  
4 cycle type, a routing field and a layer field.

1           11.   A method according to claim 10 wherein said  
2 control fields of said left source and said right source  
3 are combined to assign a single set of control fields to  
4 the resulting sum from said adder and control device.

1           12.   A method according to claim 9 wherein said zero  
2 value is selected as said right source if said left source  
3 is to pass-through said adder and control device.

1           13.   A method according to claim 1 wherein said  
2 initial input values are floating point in nature.

14. A method of accumulating initial input values from an arbitrary N-length string, said method simulating a layered tree structure, comprising:

- streaming said initial input values in their original order;
- selecting a left side source and a right side source, said selection made from among a zero value, said initial input values and a set of intermediate result values;
- adding said left side source and said right side source to generate an adder output value;
- and directing said adder output value to one of a memory bank and a result queue, each said adder output value directed to said memory bank a member of said set of intermediate result values and each said adder output value directed to said result queue, the final result of accumulating all N said initial input values, wherein the order of adding is maintained within each said layer.

15. A method according to claim 14 wherein streaming includes:

- counting the phase of each initial input;
- passing directly without delay those initial inputs having an odd phase count; and

6       delaying initial inputs having an even phase count,  
7       further wherein said delaying is such that said initial  
8       inputs having an even phase count are available to be  
9       accumulated contemporaneously with said initial inputs  
10      having an odd phase count.

1       16. A method according to claim 15 further comprising:  
2       assigning a set of control fields to each initial  
3       input value and to each adder output result value.

1       17. A method according to claim 16 wherein assigning  
2       includes:

3       combining said control fields of said left source with  
4       the control fields of said right source according to a set  
5       of rules, the set of control fields resulting from said  
6       combining being assigned to said adder output result value.

1       18. A method according to claim 17 wherein said  
2       control fields include a cycle type, a routing field and a  
3       layer field.

1       19. A method according to claim 18 wherein said cycle  
2       type is one of a Start, End, Normal and Done types.

1        20. A method according to claim 18 further  
2 comprising:  
3        partitioning said memory bank into a right memory and  
4 left memory bank, each partition representing branches of  
5 said layered tree to right and left directions,  
6 respectively.

1        21. A method according to claim 20 wherein  
2 partitioning includes:  
3        segregating said right memory bank into FIFOs, the  
4 FIFOs equal to the number of operational layers desired in  
5 said layered tree being simulated; and  
6        segregating said left memory bank into FIFOs, the  
7 FIFOs one more than the number of operational layers  
8 desired in said layered tree being simulated.

1        22. A method according to claim 21 wherein said each  
2 FIFO of said left memory bank represents one of said  
3 operational layers and a bridge layer of said layered tree.

1        23. A method according to claim 21 wherein said each  
2 FIFO of said left memory bank represents one of said  
3 operational layers of said layered tree.

1        24. A method according to claim 23 wherein said  
2 routing field includes indications of which one of said  
3 FIFOs, at each layer, the data that accompanies it belongs.

1        25. A method according to claim 23 wherein said left  
2 and right source are at the same operational layer when  
3 being added except where a bridge layer add is performed.

1        26. A method according to claim 25 wherein said  
2 length N is allowed to be arbitrarily large by performing  
3 bridge layer adds for each of said initial input values  
4 exceeding the number allowed by said operational layers.

1        27. A method according to claim 14 wherein said  
2 initial input values are floating point in nature.

1        28. An apparatus configured to simulate a layered tree  
2 structure to accumulate initial input values from arbitrary  
3 N-length string, comprising:

4        a left input selector configured to select a left  
5 input from among one said initial input value and a  
6 plurality of left-side intermediate result values;

7 a right input selector configured to select a right  
8 input from among one said initial input value and a  
9 plurality of right-side intermediate result values; and  
10 an adder and control device configured to sum together  
11 said left input and said right output, said sum determined  
12 to be either one of said left-side and right-side  
13 intermediate result values or a final output resulting from  
14 the accumulating of said N initial inputs, said adder and  
15 control device configured to direct said sum in order to  
16 maintain the order of adds within each said layer.

1 29. An apparatus according to claim 28 further  
2 comprising:

3 a left memory bank configured to store said left-side  
4 intermediate result values, wherein the input ports of said  
5 memory bank is coupled to said adder and control device,  
6 and the output ports of said memory bank are coupled to the  
7 right selection mechanism; and

8 a right memory bank configured to store said left-side  
9 intermediate result values, wherein the input ports of said  
10 memory bank is coupled to said adder and control device,  
11 and the output ports of said memory bank are coupled to the  
12 right selection mechanism.



1        30. An apparatus according to claim 29 wherein said  
2 memory banks consist of a plurality of FIFOs.

1        31. An apparatus according to claim 30 wherein the  
2 FIFOs belonging to said left memory bank include a bridge  
3 layer FIFO.

1        32. An apparatus according to claim 28 further  
2 comprising:  
3        a phase counter configured to count said initial input  
4 values and configured to output a phase value for each said  
5 initial input value.

1        33. An apparatus according to claim 32 further  
2 comprising:  
3        a delay element coupled to said phase counter and said  
4 left input selection mechanism, configured to delay said  
5 initial input values that have an even number phase prior  
6 to being input to said left selection mechanism.

1        34. An apparatus according to claim 28 further  
2 comprising a result queue, said result queue to receive

3 from the adder and control device said final output  
4 resulting from the accumulating of said N initial inputs.

1 35. An apparatus according to claim 31 wherein said  
2 left memory bank includes one FIFO for every operational  
3 layer in said tree structure.

1 36. An apparatus according to claim 35 wherein said  
2 right memory bank includes one FIFO for every operational  
3 layer in said tree structure.

1 37. A method according to claim 28 wherein said  
2 initial input values are floating point in nature.